TID Test Results of LVDS Driver and Receiver ICs with Extended Common Mode Capability

Y. Tcherniavskaya*, V. Burkhay, A. Rocke, V. Shunkov, F. Gerfers

Abstract **- This report provides results of TID robustness tests of LVDS driver and receiver. 56 krad (Si) hardness with full performance has been achieved. With certain limitations circuits are working up to 100 krad (Si).**

Index Terms* - *SpaceWire, Low-Voltage Differential Signaling (LVDS), Total Ionized Dose (TID), Space.

I. Introduction

Low Voltage Differential Signaling (LVDS) is a low power and a high-speed interface and signal transmitting technique widely used for SpaceWire applications and is absolutely essential for aerospace equipment manufacturers. Recently arose an extensive demand on radiation hard LVDS components suitable for extended common mode applications at high communication speed [9]. That would help solving some currently existing robustness issues.

The extended common mode capable LVDS components have been designed by SPACE IC GmbH. It is the combination of high-speed performance and efficiency of LVDS with the RS-485 receiver input voltage range [8]. New chips provide extended common mode capability from –7V to +12V and robust but also fast communication channels, which makes them perfect for extreme environments like space (Fig. 1).

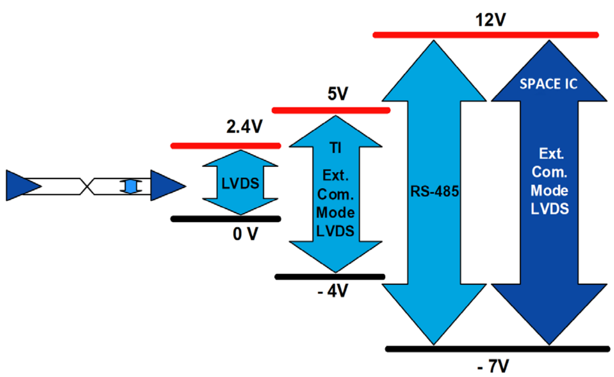


Fig. 1: Extended Common Mode LVDS

Those ICs translate the LVDS signals to 3.3V CMOS/TTL and vice versa with max provided data rate of 400Mbps and higher. The max data rate of such translators is limited by the CMOS I/O circuits.

The radiation test has been performed on two types of components (Fig. 2): transmitter SPLVDS031RH [1] and receiver SPLVDS032RH [2].

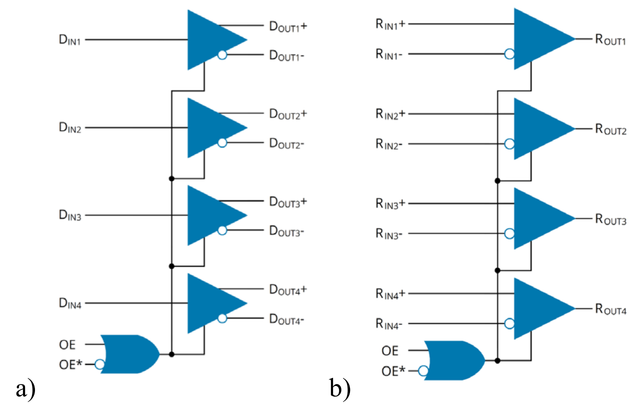


Fig. 2: Functional Block Diagram of TX [1] (a) and RX [2] (b)

The aim of this TID evaluation test campaign was to determine the TID radiation hardness level of the components in biased condition and to find the worst case LVDS TX and RX channel biasing.

II. Measurement Setup

Several radiation tests have been previously performed on both the transmitter **SPLVDS031RH** and the receiver **SPLVDS032RH**:

- SEE heavy ions test up to 65.2 MeV / (mg/cm^2);
- High dose-rate TID test up to 100krad, unbiased condition;

This test was to determine TID hardness of parts in biased condition, at dose rate 360 rad/h. Biasing circuits were implemented to keep TX and RX DUTs under four different biased states during irradiation, respectively:

1) SPLVDS031RH TX channels:
   A. HIGH input, terminated output
   B. HIGH input, non-terminated output
   C. LOW input, terminated output
   D. LOW input, non-terminated output

2) SPLVDS032RH RX channels:
   A. V_RINx = +11.5V, V_RINx = +12.5V (R_{OUT}=L or H)
   B. V_RINx = −6.5V, V_RINx = −7.5V (R_{OUT}=H or L)
   C. V_RIN+ = +1.7V, V_RIN– = +0.7V (R_{OUT}=H)
   D. V_RIN+ = open, V_RIN– = open (R_{OUT}=H)

* Y. Tcherniavskaya is with the Space IC GmbH and Technical University of Berlin, Germany; email: y.tcherniavskaya@space-ic.com
V. Burkhay, A. Rocke, V. Shunkov, are with the SPACE IC GmbH, Garbsener Landstraße 10, 30419 Hannover, Germany
F. Gerfers is with the Technical University of Berlin, Straße des 1. Juni 135, 10623 Berlin, Germany

The TID test has been executed at the ESTEC ^{60}Co Facility in Noordwijk, Netherlands. For the post-irradiation annealing phase the measurement setup was relocated to SPACE IC lab facilities in Hannover, Germany. The picture below shows the 360rad/h radiation setup with biased TID test board:

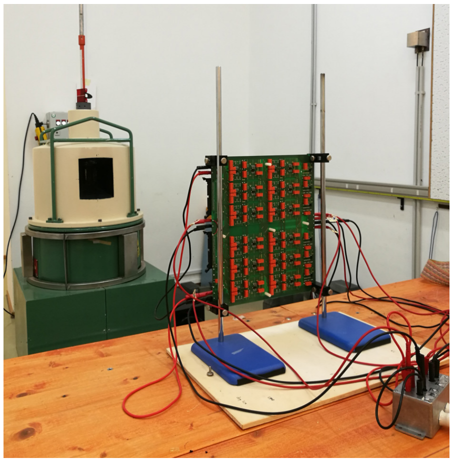


Fig. 3: TID Setup in the irradiation chamber

Output voltages and current consumption of DUTs have been continuously monitored during irradiation, while extensive measurements were performed between irradiation steps. The irradiation steps were:

TABLE I
Irradiation steps

Dose-rate	Accumulated Dose							
360 rad/h	25 krad	32 krad	40 krad	50 krad	56 krad	82 krad	90 krad	100 krad

24h room temperature annealing (RTA) under bias and 168h high temperature annealing (HTA) at 100°C under bias (accelerated ageing) followed the irradiation.

The intermediate electrical measurements, as well as initial and final ones, have been executed with an automated DC parameter measurement setup and a manual high-frequency measurement setup outside the irradiation chamber. After every irradiation step, RTA and HTA, a set of electrical parameters (TABLE II) has been measured at room temperature on a setup controlled by a LabVIEW test program.

TABLE II
Main parameters tested

TX Parameters	RX Parameters
1. Continuity	1. Continuity
2. CMOS input current	2. CMOS input current
3. Current consumption	3. LVDS input current
4. OUTx output voltages	4. Current consumption
5. DINx input threshold	5. Output high voltage
6. OE & OE* threshold voltage	6. Output low voltage
7. Output short circuit current to VCC or GND	7. Output short circuit current
8. Output high-Z current	8. Output high voltage if failsafe
9. Output differential short circuit current	9. Output high-Z current
10. Output power-off current	10. Differential input thresholds at V_{ICM} = 1.2 V / –7 V / 12V

III. TID Test results

A. *In-Situ measurement results*

1) For *SPLVDS031RH*, measured parameters were:

- output voltages of terminated outputs – H and L single-ended output state
- output common mode of terminated outputs
- output differential magnitude of terminated outputs
- output voltages of non-terminated outputs – H and L single-ended output state
- current consumption

Fig. 4 and Fig. 5 show some results of the TX monitoring during irradiation and measurements after RTA and HTA. All parts passed the 56 krad (Si) fully operational and within specifications. Above 83 krad (Si) some parts showed issues with starting up the chip-internal LVDS output reference voltage. This effect leads to a reduced output common mode and magnitude violating the LVDS driver specification. Nevertheless, the components remain functional with good dynamic performance (see eye diagrams in the TABLE III).

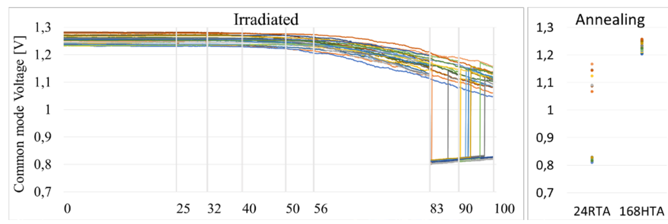


Fig. 4: Common mode of channels with terminated TX output [3]

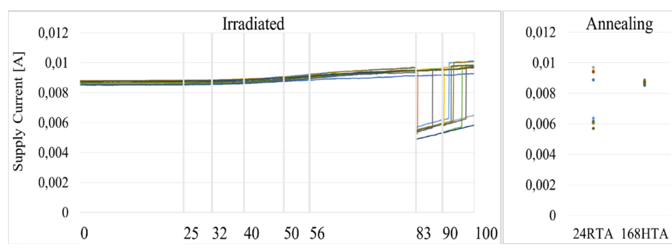


Fig. 5: Supply current of TX samples [3]

2) For *SPLVDS032RH*, measured parameters were:

- output voltages for H input signal
- output voltages for L input signal
- current consumption

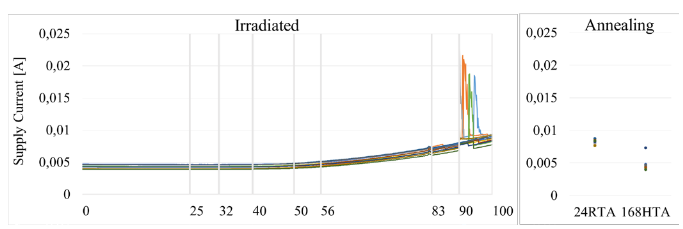


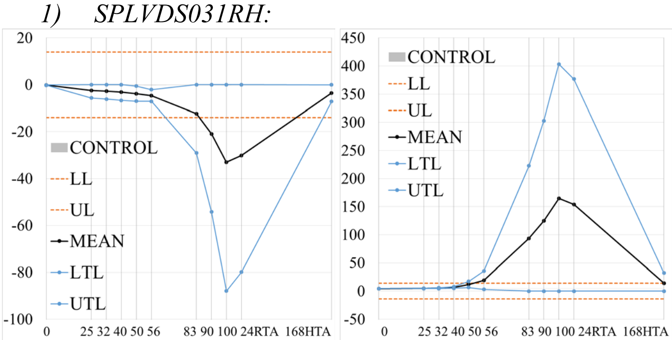
Fig. 6: Supply current of RX samples [4]

Fig. 6 shows one of the RX monitoring data (Supply current) during irradiation and measurements after RTA and HTA. All parts passed the 56 krad (Si) fully operational and within specification. Above 83 krad (Si) the parts lost extended common mode capability. This resulted in output signal failures for the channels A and B biased at –7 V and +12 V common mode respectively. Temporary increases in current consumption indicate oscillations where degraded input threshold voltages at extreme common modes came close to the applied input signals.

B. Intermediate measurement results

The analysed data contains the mean value, standard deviation and the mean value with the KTL value (one-sided tolerance limit) applied: lower tolerance limit LTL = MEAN – KTL x SIGMA and upper tolerance limit UTL = MEAN + KTL x SIGMA per ECSS-Q-ST-60-15C [6] and MIL-HDBK-814 [7]. The charts also show (in grey) the mean value and tolerance band of the control group. The control units show no significant changes to any of the parameters, so that means that the observed degradation was due to the radiation exposure. The behaviour during irradiation and annealing of some chosen parameters from the TABLE II are listed below.

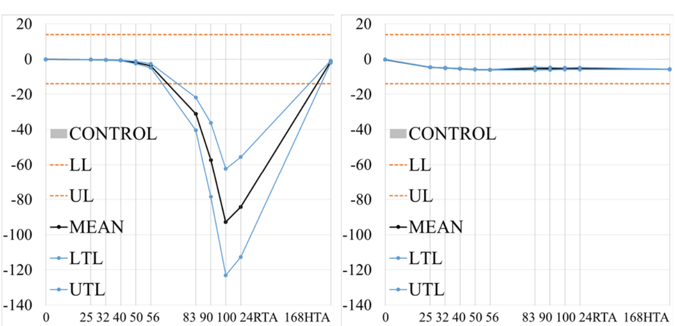
1) SPLVDS031RH:



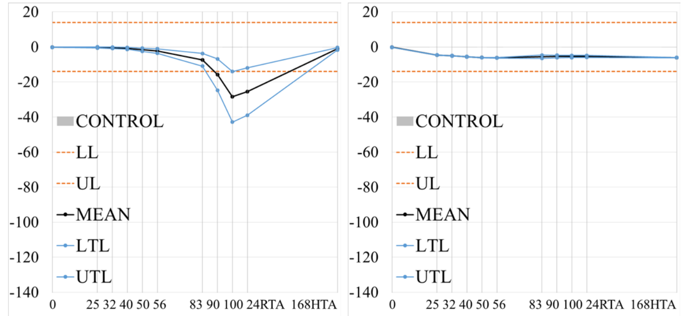
a) b)

Fig. 7: OUTx high-Z current [µA] to GND (a) and VCC (b) [3]

Fig. 7 shows the TX parameter Output High Impedance Current, shorted to VCC and GND. A correlation with the output voltage biasing (**H**igh voltage and **L**ow voltage in the Fig. 8 and Fig. 9) and termination state (term/non-term) has been observed. For a differential output interface one pin will always be High and the other pin Low. Therefore, the bias worst cases are *static terminated* for high-Z current to GND and *static non-terminated* for the high-Z current to VCC (independent of the input signal state). The best case is DC-balanced signal output without and with termination respectively.



a) b)



c) d)

Fig. 8: Correlation of OUTx high-Z current [µA] to GND: H term (a), L term (b), H open (c) and L open (d) [3]

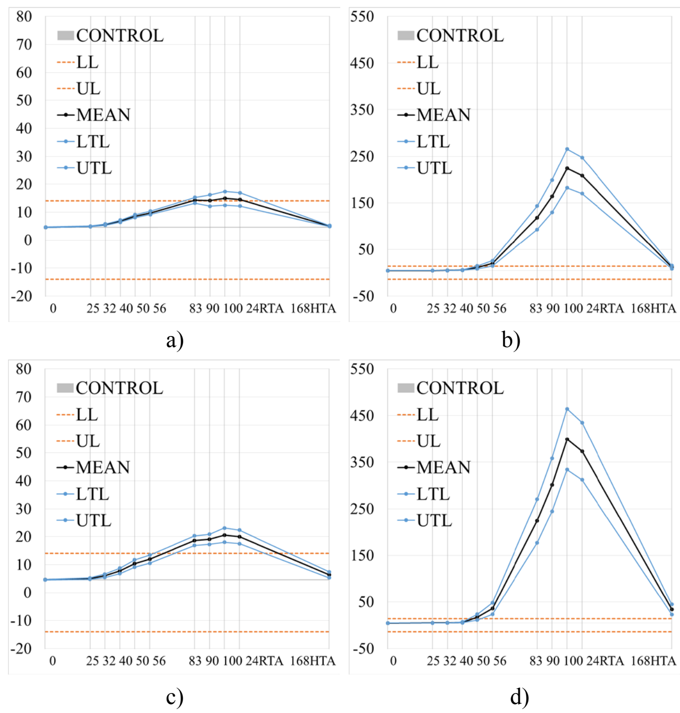
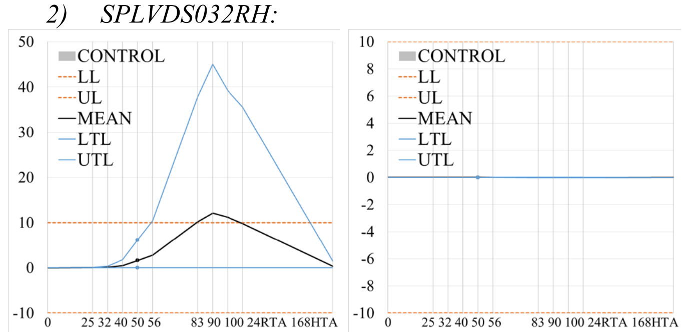


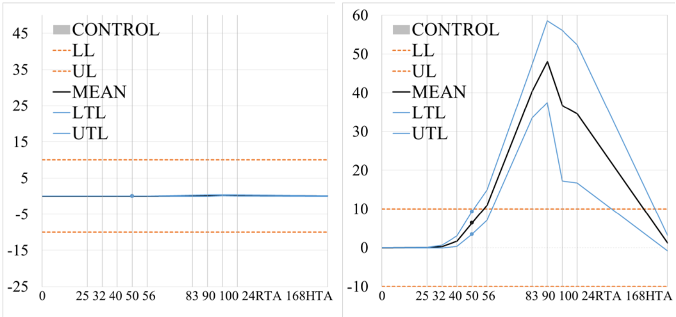
Fig. 9: Correlation of OUTx high-Z current [µA] to VCC: H term (a), L term (b), H open (c) and L open (d) [3]

2) SPLVDS032RH:



a) b)

Fig. 10: Output disable current [µA], short to VCC (a) and GND (b) [4]



a) b)

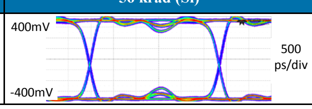
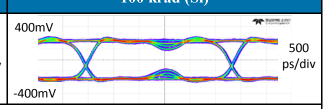
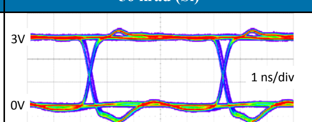
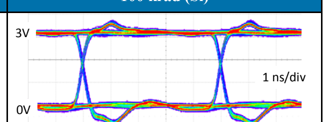
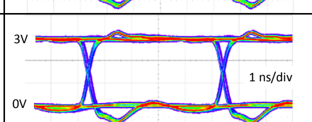
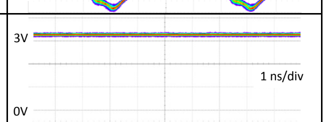
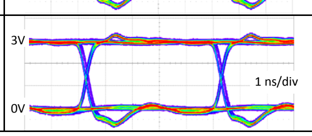
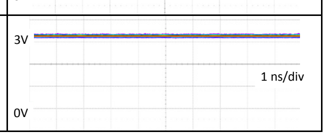
Fig. 11: Correlation of output disable current [µA] with output state during irradiation: H (a) and L (b) [4]

Fig. 10 shows the RX parameter Output disable current shorted to VCC and GND. A correlation with the output state shows only Output disable current shorted to VCC (Fig. 11), where the worst case bias is the biasing with Low output state.

C. High-Frequency measurement results

Additionally the high-frequency performance of the components was tested. The eye diagrams of some ICs and channels are shown below.

TABLE III
Eye Diagrams of one channel of TX [3] and RX [4] (at 3 common modes)

TX, channel A		
Total Dose	**56 krad (Si)**	**100 krad (Si)**
		
RX, channel A		
Total Dose	**56 krad (Si)**	**100 krad (Si)**
CM 1.2 V		
CM 12 V		
CM –7 V		

The eye diagram showed good device performance up to 56 krad (Si). After 83 krad (Si) the TX components continued to function with good dynamic performance but with reduced amplitude. The RX components with standard common mode continued to function properly up to 100 krad (Si), whereas the ECM regulation only till 56 krad (Si).

VI. SUMMARY

The SPLVDS031RH and the SPLVDS032RH components can be considered as class F (50 krad). They operate with full performance up to 56 krad (Si). The TID threshold is between 56 krad (Si) and 83 krad (Si). Above this threshold some parameters are violated, which is usually power consumption and leakage currents, although until 100 krad (Si) components can be used with good dynamic performance (see eye diagrams) with certain limitations: TX components violate the LVDS output voltage specifications (drop in magnitude and common mode), while the Rx components with standard common mode (1.2V) continue to function properly but lose the Extended Common Mode capability.

The goal of current testing was also to evaluate the dependencies of irradiation degradation on biasing conditions, such as different input and output states and terminations, to identify the worst-case bias condition. For the relevant parametric degradations they are:

1) *For SPLVDS031RH*

- OUTx high-Z current to GND – static, terminated
- OUTx high-Z current to VCC – static, non-terminated
- OUTx power-off output current – static, non-terminated

2) *For SPLVDS032RH*

- OUT disable current, short to VCC – L output state

All parameter drifts induced by irradiation recovered under annealing.

Results have been studied for future device improvements.

ACKNOWLEDGEMENT

We are deeply thankful to ESA/ESTEC for providing us with the opportunity of holding this TID test. We express our special gratitude to ^{60}Co Facility team: Michele Muschitiello (Senior Component Engineer at ESA/ESTEC) and Alessandra Costantino (TEC-QEC Radiation Test Engineer at ESA/ESTEC) for their support and help in radiation laboratory during the test.

REFERENCES

[1] **SPACE IC** (2014): “Preliminary Datasheet SPLVDS031RH, Quad LVDS Line Transmitter”.

[2] **SPACE IC** (2014): Preliminary Datasheet SPLVDS032RH, Quad LVDS Line Receiver with Extended Common Mode.”

[3] **SPACE IC** (2019): “ECM LVDS031 TID Evaluation Testing Report”.

[4] **SPACE IC** (2019): “ECM LVDS032 TID Evaluation Testing Report”.

[5] **ESA** (June 2016): “ESCC Basic Specification No. 2290 - Total Dose Study - State Irradiation Test Method”.

[6] **ESA-ESTEC** (2012). “Space product assurance, Radiation hardness assurance - EEE components, ECSS-Q-ST-60-15C”.

[7] **MIL-HDBK-814** (1994): “Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices”.

[8] **V. Burkhay, A. Rocke, G. Magistrati, G. Furano, F. Guettache**, “Radiation-Tested Extended Common Mode LVDS Components”, 6th International SpaceWire Conference, Athens, September 2014

[9] **J. Ilstad**, “ESA’s Requirements for future LVDS devices”, LVDS Application Workshop, Noordwijk, June 2011