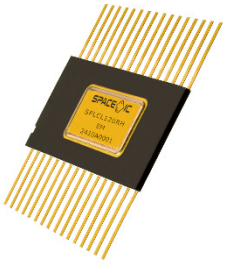
SPLCL120RH



Rad-Hard Versatile Latching Current Limiter Controller IC

FEATURES

- Electronic power bus protection
- Adjustable current class
- Bus voltage up to 120 V
- Double bus isolation
- Low power consumption
- Integrated power supply with charge pump
- Supports any kind of enhancement-mode (normally OFF) n-Channel FETs as Power Switch for high efficiency
- Adjustable GATE control voltage range
- Bi-directional Electronic Fuse
- Adjustable trip-off time
- Adjustable re-triggering / period
- Adjustable bus under-voltage and hysteresis
- Adjustable external over-temperature
- Adjustable output power good threshold
- Status telemetry (4x outputs)
- Transconductance amplifier for high stability and smooth GATE regulation
- Adjustable derivative gain
- SPI interface for redundant TM, TC, optional settings and ADC measurements
- ADC for output current, ext. power switch temperature and voltage drop telemetry
- LDR TID > 100 krad (Si)
- SEE tolerant LET ≤ 60 MeV·cm^2/mg Latch-up immune (fully isolated SOI technology)
- Screened according to ESCC
- Extended temperature range: −55 °C to +125 °C

APPLICATIONS

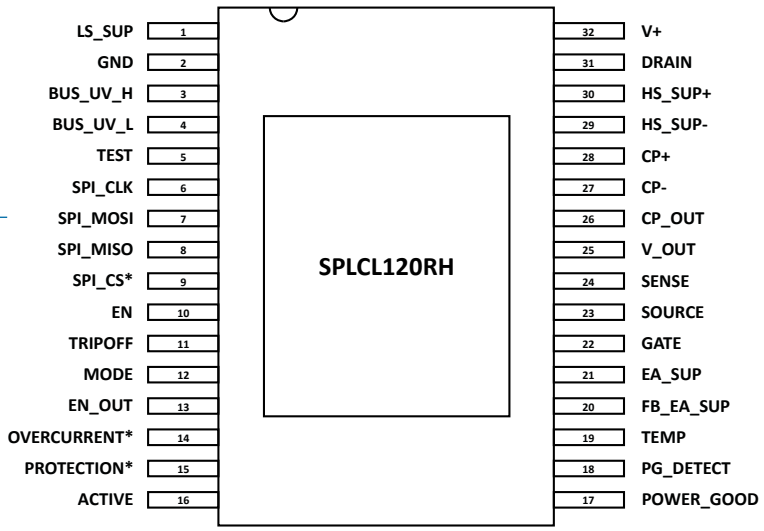
- Spacecraft power systems
- Re-configurable power protection
- Power Conditioning and Distribution Units
- Secondary power distribution
- Power rail protection
- Latch-up protection
- Current limiters
- Power telemetry

DESCRIPTION

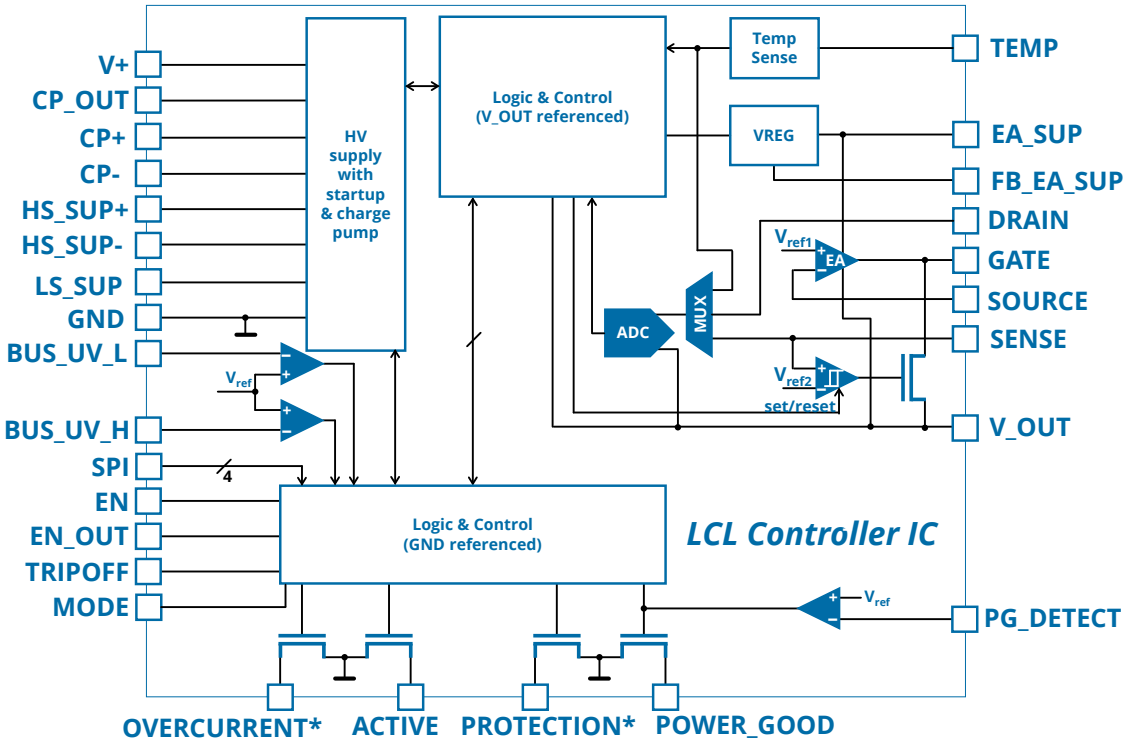
The SPLCL120RH is a radiation hardened integrated circuit for a convenient creation of re-configurable electronic power bus protection functions for space applications. It supports a high number of different configurations as Latching Current Limiter, Circuit Breaker, Electronic Fuse or simple Power Switch. Only some passive external components and an enhancement-mode (normally OFF) n-Channel FET are required to build these functions.

The SPLCL120RH can be operated at input voltages up to 120 V. An external current sense resistor between SENSE and V_OUT sets the current class. Once the output current reaches 125% of its settable nominal value the output current limitation can start. After the expiration of a programmable trip-off time or when the current reaches 400% of the default nominal output current the LCL controller turns off the external power switch. It can re-activate the output after a programmable re-triggering period. By disabling the current limitation feature the controller can be used to build an electronic fuse or circuit breaker.

PIN DIAGRAM



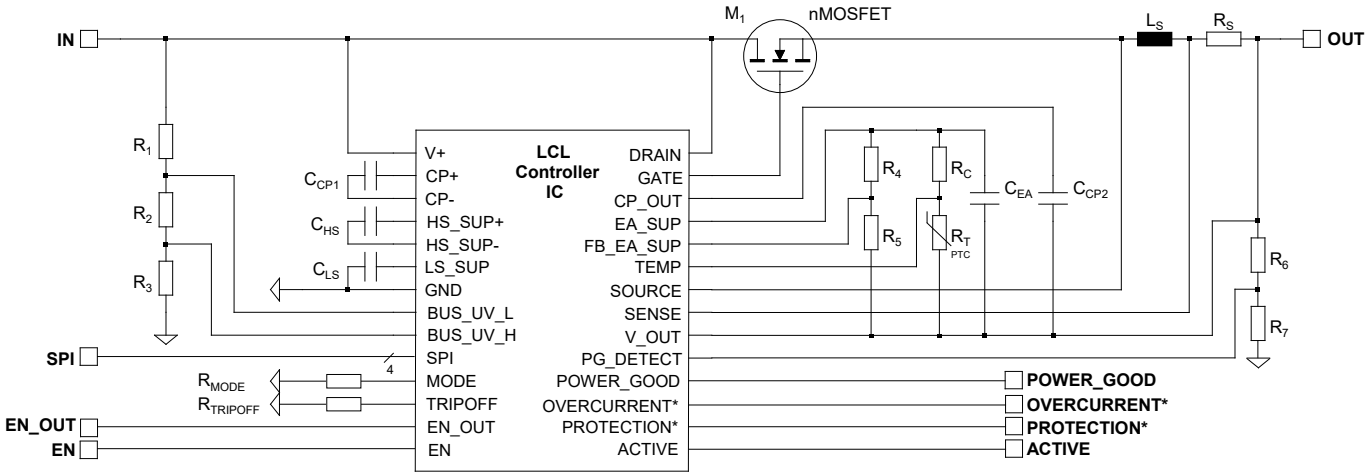
FUNCTIONAL BLOCK DIAGRAM



NOTE:

V_{ref}	comparator detection threshold
V_{ref1}	error amplifier reference for current regulation and trip-off time counting
V_{ref2}	gate switch comparator reference for fast trip-off

TYPICAL APPLICATION



PIN DESCRIPTIONS

PIN NAME	PIN #	PIN DESCRIPTION
LS_SUP	1	Positive voltage terminal for the external low side supply capacitor.
GND	2	Ground connection for chip internal low side circuitry.
BUS_UV_H	3	Negative input terminal for upper limit bus under-voltage comparator.
BUS_UV_L	4	Negative input terminal for lower limit bus under-voltage comparator.
TEST	5	This pin is for test purpose only. Connect to GND for application.
SPI_CLK	6	Clock input pin for digital SPI interface.
SPI_MOSI	7	Digital SPI interface data input pin.
SPI_MISO	8	Digital SPI interface data output pin. Open-drain output.
SPI_CS*	9	Digital SPI interface chip select input pin, active Low. Internal pull-up.
EN	10	Enable input of internal circuitry. The High level on this pin enables the chip. The Low level on this pin puts the chip into a low-power mode.
TRIPOFF	11	Trip-off duration setting: Connect a resistor in the range of 200 kΩ to 10 kΩ from TRIPOFF interface to GND interface to set the desired tripoff duration between 20ms and 1ms. Connect the TRIPOFF pin to ground to set the tripoff duration to the internal default of 1ms. By leaving the TRIPOFF interface open or connection to the LS_SUP pin the current threshold at 125% of the nominal current can be disabled (electronic fuse mode).
MODE	12	Re-trigger functionality and circuit breaker configuration: Connect a resistor in the range of 200 kΩ to 10 kΩ from MODE interface to GND interface to set the retrigger interval between 80s and 4s. Connect this pin to ground to disable the retrigger functionality. Leaving this pin open or connection to the LS_SUP pin will disable the output regulation (circuit breaker mode).
EN_OUT	13	Output enable. A High level on this pin switches on the LCL output.
OVER CURRENT*	14	Open-drain status output which asserts Low to flag an overcurrent event: - Load was disconnected due to end of trip-off timer or 400% current limit - The output current exceeds currently 125% of the nominal value
PROTECTION*	15	Open-drain output which asserts Low to flag that the load was disconnected because of one of the following protection reasons: - 400% current limit - Over-temperature of either power switch or controller IC
ACTIVE	16	Open-drain active output which asserts High to flag that the output is enabled.
POWER_GOOD	17	Open-drain power good output which asserts High if the output voltage is higher than the voltage threshold programmed by PG_DETECT.
PG_DETECT	18	Positive input terminal for lower limit output voltage comparator. Used to set the threshold for output voltage where POWER_GOOD will be raised.
TEMP	19	The TEMP pin is used to connect to a combination of thermistor and resistor between EA_SUP and V_OUT to enable temperature sensing of the external transistor. Connecting this pin to V_OUT will disable temperature sensing.
FB_EA_SUP	20	GATE control voltage range setting: Connect this feedback pin to a voltage divider between EA_SUP and V_OUT to set the desired EA_SUP voltage in order to adjust the nominal power switch gate control voltage.

The asterisk (*****) at the end of the pin name means inverted pin logic: Low = TRUE and High = FALSE

PIN DESCRIPTIONS (CONTINUED)

PIN NAME	PIN #	PIN DESCRIPTION
EA_SUP	21	Output of the linear regulator supplying the error amplifier of the current control loop. Needs to be bypassed to V_OUT by an external capacitor.
GATE	22	Power Switch gate connection interface. This pin is driven by the output of the current control loop error amplifier.
SOURCE	23	Connect this pin to the source of the external power switch. Negative input terminal of current control loop error amplifier.
SENSE	24	Current sensing: Connect a current sense resistor between this pin and V_OUT to set the current class. The voltage drop is 100mV at nominal current.
V_OUT	25	Output voltage of the LCL. A current sense resistor needs to be connected between this pin and SENSE. While the output voltage is over a certain limit the chip consumes current from this node for the internal circuitry.
CP_OUT	26	Output of the internal charge pump. Needs to be bypassed to V_OUT by an external capacitor.
CP-	27	Negative voltage terminal for the external charge pump capacitor.
CP+	28	Positive voltage terminal for the external charge pump capacitor.
HS_SUP-	29	Negative voltage terminal for the external high side supply capacitor.
HS_SUP+	30	Positive voltage terminal for the external high side supply capacitor.
DRAIN	31	Power switch drain connection interface. This pin is used to measure the voltage drop over the power switch.
V+	32	The V+ input is used as a start-up power source and when the V_OUT voltage is not high enough to supply the internal voltage regulators.

STATUS OUTPUT STATES

CONDITION	ACTIVE	POWER_GOOD	OVERCURRENT*	PROTECTION*	COMMENTS
Controller IC disabled by user (shut down)	H	H	H	H	EN=L
Output disabled by user	L	X	H	H	EN=H; EN_OUT=L
Nominal operation, $V_{OUT} < V_{th,PG}$	H	L	H	H	only during start-up or in case of $V_{BUS} < V_{th,PG}$
Nominal operation, $V_{OUT} > V_{th,PG}$	H	H	H	H	EN=H; EN_OUT=H
Output enabled, current limitation	H	X	L	H	EN=H; EN_OUT=H
Output protection after trip-off	L	X	L	H	EN=H; EN_OUT=H
Output protection by the 2nd current limit	L	X	L	L	EN=H; EN_OUT=H
Output protection by over-temperature	L	X	H	L	EN=H; EN_OUT=H

OPERATING CONDITIONS

All voltages with respect to GND / AGND, unless otherwise specified. Typical values at TA = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{V+,OP}$	V+ supply voltage		14	28	120	V
V_{LS_SUP}	LS_SUP supply voltage		10		28	V
V_{EA_SUP}	EA_SUP supply voltage	by R_4 and R_5, to V_OUT	4.5		16	V
C_{CP1}	CP capacitor		10		100	nF
C_{CP2}	CP_OUT capacitor		100		200	nF
C_{LS}	LS_SUP capacitor		0.5	1	2	µF
C_{HS}	HS_SUP capacitor		100		200	nF
C_{EA}	EA_SUP capacitor		100		200	nF
R_4	FB_EA_SUP resistor			10		kΩ
C_{V_OUT}	V_OUT capacitor				10	nF
L_{V_OUT}	V_OUT inductor		0.3		300	µH
C_{GATE}	Gate capacitance				10	nF
R_{MODE}	MODE resistor		10	30	200	kΩ
$R_{TRIPOFF}$	TRIPOFF resistor		10	30	200	kΩ
C_{par}	MODE, TRIPOFF cap.	parasitic capacitance			1	nF
$T_{J,OP}$	Junction temperature		-55	27	125	°C

PARAMETERS

All voltages with respect to GND / AGND, unless otherwise specified. Typical values at TA = 25 °C.

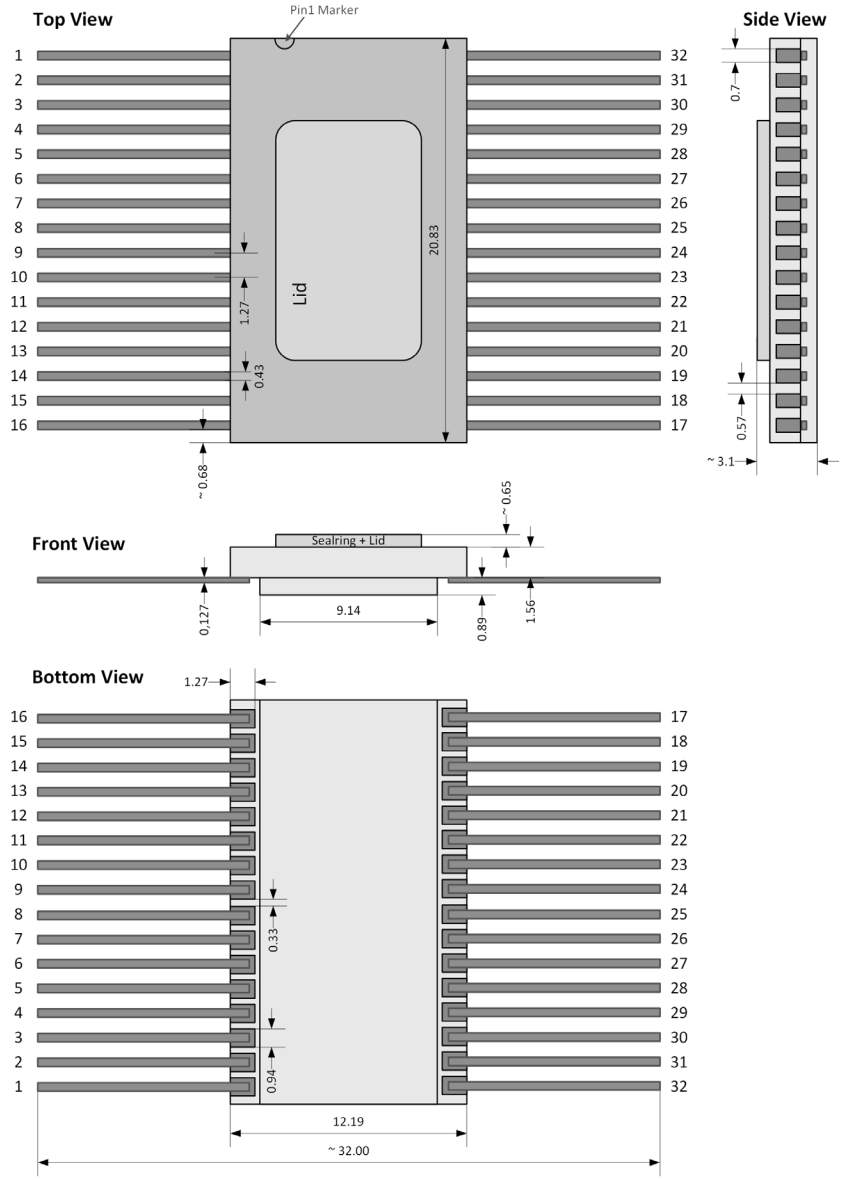
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{V+,SD}$	Shutdown supply current V+	EN=L		0.16	0.2	mA
$I_{V+,OFF}$	OFF supply current V+	EN=H; EN_OUT=L		0.7	1	mA
$I_{GND,ON}$	ON supply current (GND)	EN=EN_OUT=H		2.2	3	mA
Control Inputs EN, TEST						
$V_{H,th}$	H threshold	rising	0.67	0.69	0.7	V
$V_{L,th}$	L threshold	falling	0.59	0.6	0.61	V

PARAMETERS (CONTINUED)

All voltages with respect to GND / AGND, unless otherwise specified. Typical values at TA = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Control Input EN_OUT						
$V_{H,th}$	H threshold	rising	0.97	0.99	1.02	V
$V_{L,th}$	L threshold	falling	0.88	0.91	0.93	V
Error Amplifier Supply						
V_{FB}	FB_EA_SUP feedback voltage			1		V
Transconductance Error Amplifier						
GBW	Gain Bandwidth Product		22	56	102	Hz
$V_{EA,Offs}$	Input offset voltage				2	mV
G_{EA}	Transconductance		150	180	210	µA/V
A_{EA}	Open loop gain		27	33	40	dB
V_{ref1}	EA reference	to V_OUT	121	124	128	mV
GATE Switch Comparator						
$V_{SENSE,OVth}$	SENSE threshold	to V_OUT		400		mV
$t_{VGate,pd}$	Hold time	unlatched		64		µs
$I_{Gate,pd}$	Switch current capability			1		A
Timers						
t_{MODE}	Re-trigger period range	R_{MODE} = 10...200 kΩ	4		80	s
t_{TRIP}	Trip-off time range	$R_{TRIPOFF}$ = 10...200 kΩ	1		20	ms
Comparators						
$V_{BUS,UVth}$	BUS_UV_L/H threshold			1		V
$t_{BUS,min}$	Min. BUS event duration			1		ms
$V_{PG,th}$	PG_DETECT threshold			1		V
$V_{TEMP,th}$	TEMP shutdown threshold	to V_OUT		400		mV
Open Drain Outputs ACTIVE, OVERCURRENT*, PROTECTION*, POWER_GOOD						
$I_{OD,ON}$	OD output current	V_{OD} = 0.4...20 V	4.3	6.2	9.6	mA
$I_{OD,OFF}$	OD leakage current	V_{OD} = 30 V		2.5	400	nA
Thermal Shutdown						
T_{SD}	Thermal shutdown	internal		168		°C

PACKAGE DRAWING (32-LEAD FLATPACK)



IMPORTANT NOTICE