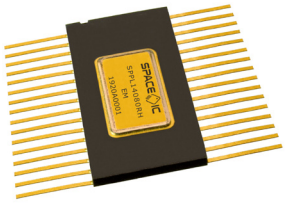
SPPL14080RH



8 A, 40 V Synchronous Rectified Step-Down Converter

FEATURES

- 8 A continuous output current
- Input voltage capability (derating reference): 40 V
- Minimum input voltage: 3.0 V
- Minimum output voltage: 0.8 V
- LDR TID > 100 krad (Si)
- Latch-up immune (fully isolated SOI technology)
- Hermetic dual in-line 32-lead flatpack package
- Screened according to ESCC
- High, >90%, efficiency (V_{IN} = 12 V, 1 A < I_{LOAD} < 6 A)
- Adjustable 100 kHz to 1 MHz frequency externally synchronizable
- 3 µA (MAX) shut-down supply current
- Programmable soft-start, cycle-by-cycle over-current protection and input under-voltage lockout
- Extended temperature range: -55 °C to +125 °C

APPLICATIONS

- High-Density Point-of-Load Regulators
- Distributed Power Systems
- Satellite Systems
- Launch Vehicles

DESCRIPTION

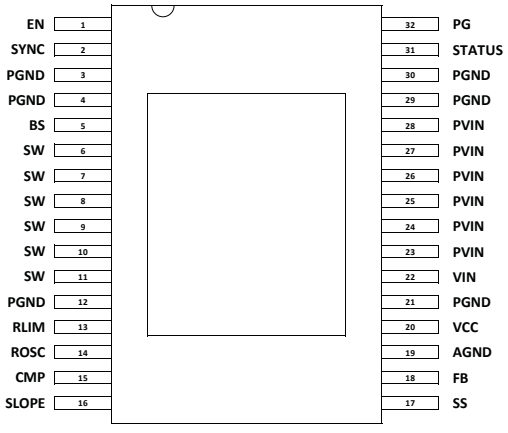
The SPPL14080RH is a radiation hardened monolithic synchronous buck regulator optimized for space and component saving board designs by featuring integrated MOSFETs that provide continuous 8 A output load current and low external component count. Its current mode control circuitry provides fast transient response and cycle-by-cycle current limit.

The SPPL14080RH can be operated at input voltages up to 40 V, which is the derating reference. The switching frequency can be controlled by an external signal through the sync pin or be set to a constant frequency between 100 kHz and 1 MHz.

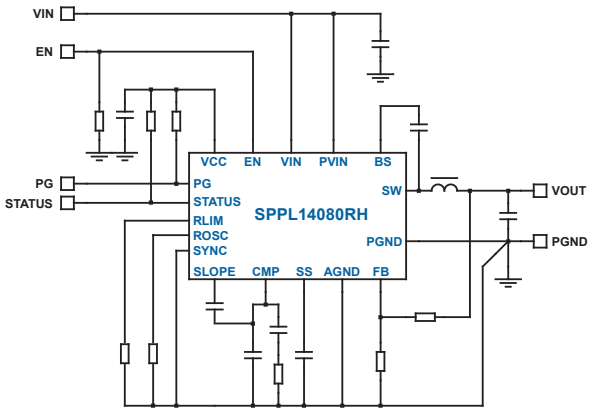
It features programmable soft-start which prevents in-rush current at turn-on. The regulator can be switched on and off via the enable pin and features a power-good output.

The device is packaged in a hermetically sealed 32-pin flatpack with heatsink and straight leads.

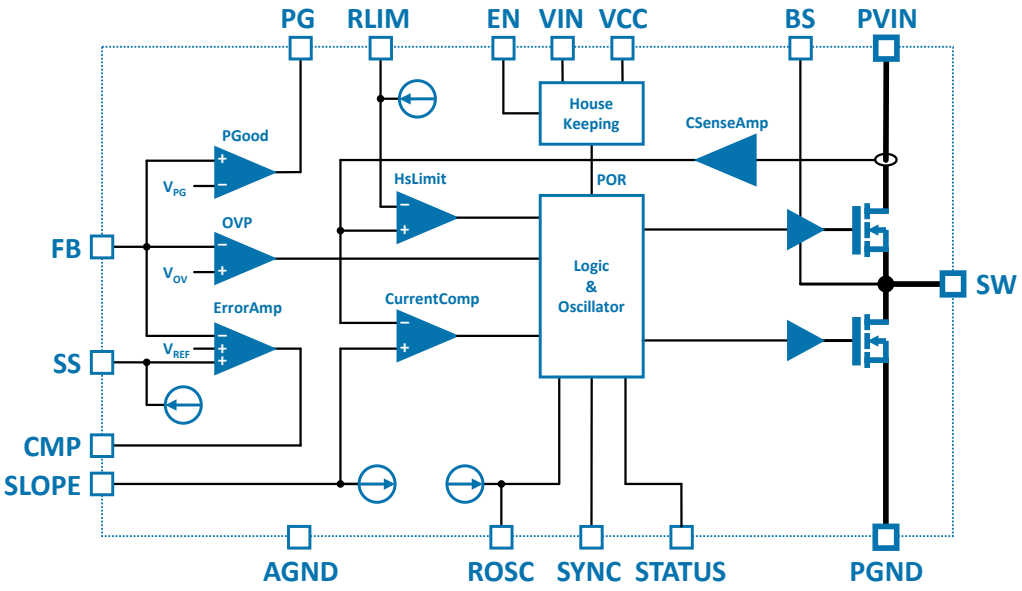
PIN DIAGRAM



TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN DESCRIPTION
EN	1	Enable input pin: The EN pin is an input pin that enables or disables the regulator. The pin has an internal pull-up. For automatic start up, leave this pin unconnected. Set the EN pin to AGND to turn the regulator off. To implement power-supply sequencing EN can be controlled by the power-good PG output of a primary device.
SYNC	2	I/O pin: Input operation: Apply a clock signal for synchronisation. A frequncy setting resistor at ROSC is mandatory for this. Output operation: If no clock is applied to this pin during startup, the pin is switched to output and the inverted clock will be available. Connect this pin to AGND to deactivate the synchronisation function completely.
PGND	3, 4, 12, 21, 29, 30	Ground pin: Heatsink and lid are connected to PGND.
BS	5	High-side gate drive boost voltage input pin: This pin supplies the driver for the high-side N-Channel MOSFET. Connect a capacitor of 0.01 µF or greater from SW to BS to power up the high-side switch.
SW	6 - 11	Power switching output pin: This pin is the switching node that supplies power to the output and toggles between PVIN and PGND voltage. Connect an LC filter between SW pin and the output load.
RLIM	13	High-side current limit setting: Connect a resistor from RLIM pin to the AGND pin to set the high-side current limit. Shorting the pin to VCC sets the limit to 6 A. By shorting this pin to AGND, the limit is set to 10 A.
ROSC	14	Oscillation frequency setting: Connect a resistor from ROSC pin to the AGND pin to set the oscillation frequency. Shorting the pin to VCC sets the frequency to 500 kHz. By shorting this pin to AGND, the regulator uses only the clock applied to SYNC for operation.
CMP	15	Compensation input pin: This pin is used to compensate the regulation control loop. Connect a series RC filter from CMP to AGND pin to compensate the regulation loop. In some cases, an additional capacitor is needed.

PIN DESCRIPTIONS (CONTINUED)

PIN NAME	PIN NUMBER	PIN DESCRIPTION
SLOPE	16	Slope compensation pin: Connect a slope compensation capacitor between CMP and SLOPE. This capacitor is charged by an internal 10 µA current to add a slope to the regulation. The slope voltage is compared with high-side current by the PWM comparator. The capacitor becomes discharged when the high-side transitor is switched off.
SS	17	Soft-start control input pin: This pin controls the soft-start period. Connect a capacitor from the SS pin to the AGND pin to set the soft-start period.
FB	18	Feedback input pin: The FB pin senses the divided output voltage to regulate that voltage. Drive the FB pin with a resistive voltage divider from the output voltage. The feedback threshold is 800 mV.
AGND	19	Analog ground pin: To be used according to typical application circuit only.
VCC	20	2.8 V I/O pin of internal regulator: Connect a 10 µF low ESR capacitor to AGND.
VIN	22	Power input pin: The VIN pin supplies the input voltage to the internal supply. Drive the VIN pin with a 3.3 V to 40 V power source. Bypass the VIN pin to PGND pin with an appropriate large capacitor to minimize noise and ripple on the input to the device.
PVIN	23 - 28	Power input pin: The PVIN pin supplies the step-down converter power MOSFETs. Drive the PVIN pin with a 3.3 V to 40 V power source. Bypass the PVIN pin to PGND pin with an appropriate large capacitor or LC-Filter to minimize noise and ripple on the input to the device.
STATUS	31	Status pin: Open-drain output which asserts low to flag following errors: Thermal shutdown, failure of ROSC resistor, high-side over-current,
PG	32	Power-good pin: Open-drain output which asserts low if the output voltage is low due to enable off, ongoing soft-start, input undervoltage lockout or thermal shut-down.