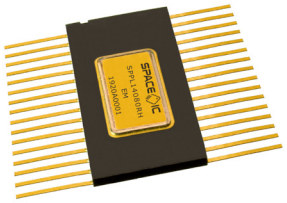
SPPL14080RH



8 A, 40 V Synchronous Rectified Step-Down Converter

FEATURES

- 8 A continuous output current
- Input voltage capability (derating reference): 40 V
- Minimum input voltage: 3.0 V
- Minimum output voltage: 0.8 V
- LDR TID > 100 krad (Si)
- Latch-up immune (fully isolated SOI technology)
- Hermetic dual in-line 32-lead flatpack package
- Screened according to ESCC
- >90% efficiency (V_{IN} = 12 V, V_{OUT} = 3.3 V, 1 A < I_{LOAD} < 6 A)
- Adjustable frequency 100 kHz to 1 MHz, externally synchronizable
- 80 µA shut-down supply current
- Programmable soft-start, cycle-by-cycle over-current protection and input under-voltage lockout
- Extended temperature range: -55 °C to +125 °C

APPLICATIONS

- High-Density Point-of-Load Regulators
- Distributed Power Systems
- Satellite Systems
- Launch Vehicles

DESCRIPTION

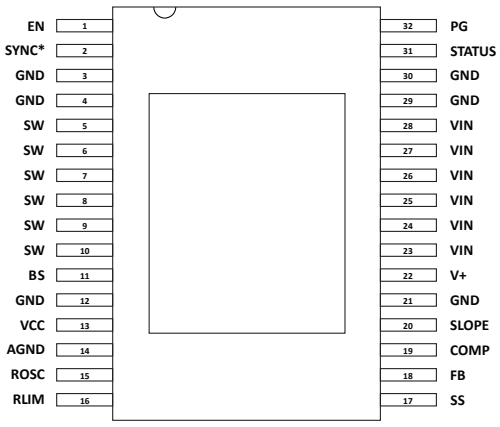
The SPPL14080RH is a radiation hardened monolithic synchronous buck regulator optimized for space and component saving board designs by featuring integrated MOSFETs that provide continuous 8 A output load current and low external component count. Its current mode control circuitry provides fast transient response and cycle-by-cycle current limit.

The SPPL14080RH can be operated at input voltages up to 40 V, which is the derating reference. The switching frequency can be set to a constant frequency between 100 kHz and 1 MHz. In addition, it can be synchronised to a clock signal applied externally to the SYNC* pin.

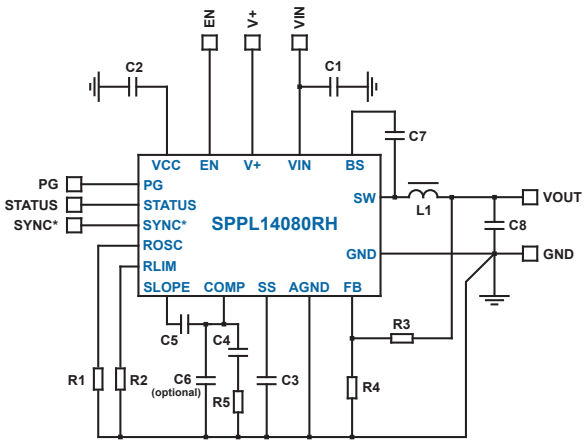
It features programmable soft-start which prevents in-rush current at turn-on. The regulator can be switched on and off via the enable pin and features power-good and status outputs.

The device is packaged in a hermetically sealed 32-pin flatpack with heatsink and straight leads.

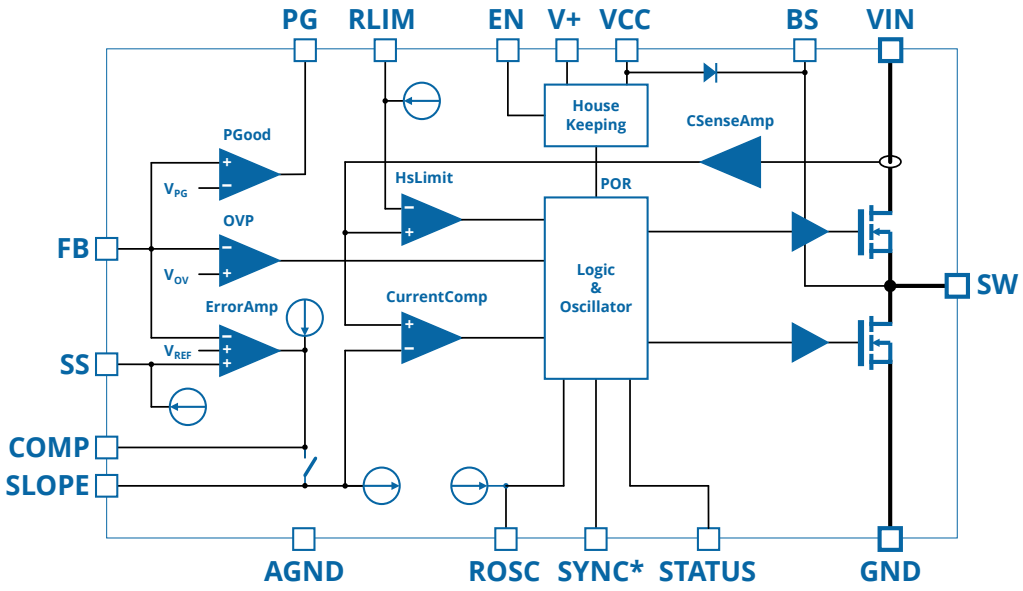
PIN DIAGRAM



TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN DESCRIPTION
EN	1	Enable input pin: It is a control input that enables or disables the regulator. The pin has an internal pull-up. For automatic start up, connect this pin to V+. Set the EN pin to GND to turn the regulator off. To implement power-supply sequencing EN can be controlled by the power-good PG output of a previously activated device. Setting EN to GND resets the latched error state.
SYNC*	2	I/O pin: Input operation: Apply a clock signal (duty cycle 25% to 75%, the falling edge starts $t_{off,min}$) for synchronisation before enable / power-up. A frequency setting resistor at ROSC is mandatory for this. The clock frequency must stay within ±10% of the set value. Output operation: If no clock is applied to this pin during startup, the pin is switched to output and the inverted clock will be available. Connect this pin to GND to deactivate the synchronisation function completely.
GND	3, 4, 12, 21, 29, 30	Power ground pins: Source connection to the low-side power MOSFET. Heat-sink and lid are connected to GND. If possible, use the heatsink as additional power ground connection. Connect the power ground pins together and to the output capacitor by a low-impedance trace.
SW	5 - 10	Power switching output pin: This pin is the switching node that supplies power to the output and toggles between VIN and GND voltage.
BS	11	High-side gate drive bootstrap voltage supply pin: This pin supplies the driver for the high-side N-Channel MOSFET. Connect a capacitor of 0.1 µF to 1.0 µF from SW to BS to power up the high-side switch.
VCC	13	Internal 2.8 V regulator output: Connect a 10 µF to 20 µF low ESR capacitor to GND (to be connected by a separate trace to the output capacitor). The maximum external load current at this pin is 10 mA.
AGND	14	Analog ground reference pin: To be used according to typical application circuit only. To be connected by a separate trace to the output capacitor.

PIN DESCRIPTIONS (CONTINUED)

PIN NAME	PIN NUMBER	PIN DESCRIPTION
ROSC	15	Oscillation frequency setting: Connect a resistor from ROSC pin to the AGND pin to set the oscillation frequency between 100 kHz and 1 MHz. Shorting the ROSC pin to AGND or to VCC sets the frequency to 1 MHz. If a clock signal is applied to SYNC* interface in this condition, the regulator uses only the clock applied to SYNC* for operation.
RLIM	16	High-side current limit setting: Connect a resistor from RLIM pin to the AGND pin to set the high-side current limit between 2A and 10A. Shorting the pin to VCC or to AGND sets the limit to 10 A.
SS	17	Soft-start control pin: This pin controls the soft-start period. Connect a capacitor from the SS pin to the AGND pin to set the soft-start period.
FB	18	Feedback input pin: The FB pin senses the divided output voltage to regulate that voltage. Drive the FB pin with a resistive voltage divider from the output voltage. The feedback target regulation value is 800 mV.
COMP	19	Compensation pin: This pin is the error amplifier output and is made available for loop compensation. Connect a series RC element from COMP to AGND pin to compensate the regulation loop. In some cases, an additional bypass capacitor is needed.
SLOPE	20	Slope compensation pin: This pin is the PWM comparator input. Connect a capacitor between COMP and SLOPE pins to add a voltage slope for slope compensation to the PWM regulation. This capacitor is charged by an internal 10 µA current. The capacitor becomes discharged when the high-side transistor is switched off. Connect COMP and SLOPE pins directly to set the slope to 0.
V+	22	Positive supply pin: The V+ pin supplies the voltage for the internal circuitry. Drive the V+ pin with a 3.0 V to 36 V power source. Bypass the V+ pin to GND (to be connected by a separate trace to the output capaciroe) with an appropriate large capacitor or LC-filter to minimize noise at the regulator supply.
VIN	23 - 28	Power input pins: The VIN connection supplies the step-down converter power MOSFETs. Drive VIN with a 3.0 V to 36 V power source. Connect the VIN pins together and bypass to GND pins with an appropriate large capacitor or LC-filter to minimize noise and ripple on the input to the device.
STATUS	31	Status pin: Open-drain output that asserts low to flag the latched errors thermal shutdown, failure of ROSC resistor or of the internal voltage reference and the non-latched overload error (2nd high-side over-current). This interface is pulled-down in shut-down state (if supplied).
PG	32	Power-good pin: Open-drain output that asserts high if the output voltage is within the defined limits. This interface is pulled-down in shut-down state (if supplied).

ABSOLUTE MAXIMUM RATINGS *(NOTE1)*

V_{VIN}, V_{V+}, V_{SYNC*}, V_{STATUS}, V_{PG}, V_{EN} ..... -0.3 V to +40 V
V_{SW} - Switch voltage ..... -1 V to V_{VIN} + 0.3 V
V_{BS} - Bootstrap voltage ..... V_{SW} - 0.3 V to V_{SW} + 4 V
All other pins ..... -0.3 V to +4 V

32-Lead Flatpack Thermal Resistance ***(NOTE2)***
θ_{JC} ..... 2 °C/W

T_L - Lead temperature (soldering, 10s) ..... +260 °C
T_{stg} - Storage temperature range ..... -65 °C to +150 °C

ESD Rating (HBM) ..... 4 kV

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
NOTE2 *When mounted on a standard JEDEC 2-layer board with bottom heatsink thermally connected.*

Recommended Operating Conditions

V_{VIN} - Input voltage ..... +3 V to +36 V
V_{V+} - Supply voltage ..... +3 V to +36 V
V_{V+} - Supply voltage (for better PSRR) ....+4.5 V to +36 V
T_A - Operating ambient temperature range ..... -55 °C to +125 °C
T_J - Operating junction temperature..... ≤ +150 °C

RADIATION HARDNESS *(NOTE3)*

LDR TID ..... > 100 krad (Si)
SEL, SEFI and SEU immune
Free from SET and destructive SEE at
LET ≤ 60 MeV·cm²/mg ..... V_{VIN}, V_{V+} ≤ 20 V

NOTE3 *For more details please request radiation report.*

ELECTRICAL CHARACTERISTICS

V_{VIN} = V_{V+} = 12 V, unless otherwise specified. Typical values at T_A = 25 °C. All voltages with respect to GND / AGND.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{SD}	Shutdown supply current	V_{EN} = 0 V		80	150	µA
I_{IN}	Supply current	V_{EN} = 2 V, V_{FB} = 1 V		7		mA
V_{FB}	Feedback voltage		0.787	0.798	0.810	V
$V_{FB,PG}$	Power good feedback voltage	PG = high	0.72		0.88	V
V_{FBth}	Feedback over-voltage threshold	V_{FB} rising	0.92	0.93	0.95	V
A_{EA}	Error amplifier voltage gain		7.08	8.91	11.22	kV/V
G_{EA}	Error amplifier transconductance	ΔI_{COMP} = 10 µA	830	1110	1270	µA / V
$R_{ON,HS}$	High-side switch ON resistance		40	46	58	mΩ
$R_{ON,LS}$	Low-side switch ON resistance		40	46	58	mΩ
$I_{OFF,HS}$	High-side switch leakage current	V_{EN} = 0 V, V_{SW} = 0 V		0.1	74	µA

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{VIN} = V_{V+} = 12 V, unless otherwise specified. Typical values at T_A = 25 °C. All voltages with respect to GND / AGND.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LIM,HS}$	Upper switch current limit	R_{LIM} = 20 kΩ	9.4	9.7	10.5	A
$I_{LIM,LS}$	Lower switch current limit	R_{LIM} = 20 kΩ	2.8	3.2	3.5	A
G_{CS}	COMP to current sense transconductance			22		A / V
I_{SLOPE}	SLOPE current		8.9	10	12.7	µA
$f_{OSC,max}$	Max. oscillation frequency	R_{OSC} = 10 kΩ	0.92	1.01	1.06	MHz
$f_{OSC,min}$	Min. oscillation frequency	R_{OSC} = 100 kΩ	89	101	114	kHz
Δf_{SYNC*}	Synchronisation clock signal frequency window	R_{OSC} = 10 ... 100 kΩ	-10		10	%
Δf_{OSC}	Oscillation frequency deviation	SYNC* signal disappeared		-20		%
$t_{OFF,min}$	Minimum OFF time	***(NOTE4)***	62	90	123	ns
$t_{ON,min}$	Minimum ON time	***(NOTE4)***	62	90	123	ns
$V_{EN,SDth}$	Enable shutdown threshold voltage	V_{EN} falling	0.59	0.61	0.62	V
$V_{EN,ONth}$	Enable start-up threshold voltage	V_{EN} rising	1.51	1.53	1.56	V
$V_{V+,LOth}$	Supply under-voltage lockout threshold voltage	V_{V+} rising	2.7	2.8	2.9	V
$V_{V+,LOhys}$	Supply under-voltage lockout threshold voltage hysteresis			100		mV
$V_{SYNC*th}$	SYNC* input threshold voltage		0.8		1.17	V
$I_{OD,ON}$	Open drain output current	V_{PG}, V_{STATUS}, V_{SYNC*} = 0.4 ... 40 V	4	6	8	mA
$I_{OD.OFF}$	Open drain leakage current	V_{PG}, V_{STATUS}, V_{SYNC*} = 40 V		40	80	nA
V_{VCC}	Output voltage of the internal regulator		2.63	2.78	2.83	V
I_{VCC}	External current consumption from the internal regulator		10			mA
I_{SS}	Soft-start current	V_{SS} = 0 V	8	10	12	µA
t_{SS}	Soft-start period	C_{SS} = 0.1 µF		8		ms
T_{SD}	Thermal shutdown	***(NOTE4)***		168		°C

NOTE4 *Not subject to production test - verified by design/characterization*

APPLICATION INFORMATION

The SPPL14080RH is a monolithic synchronous buck regulator featuring integrated 60 mΩ Power MOSFETs that can provide up to 8 A of load current. It regulates input voltages from 3 V to 40 V down to an output voltage as low as 0.8 V while providing soft-start, cycle-by-cycle over-current, under-voltage lockout and over-temperature protection.

This section of the datasheet describes typical application circuits, provides recommendations on component selection, and discusses thermal and layout design considerations.

TYPICAL APPLICATIONS

The SPPL14080RH uses a fixed frequency, current-mode step-down regulator architecture to deliver constant voltage to the load. Figure 9 shows a typical application circuit.

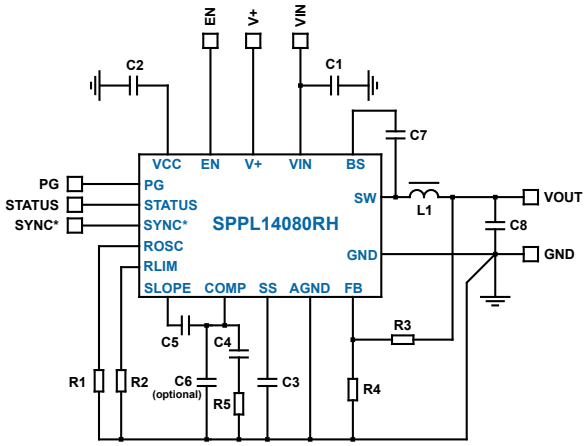


Figure 9. Typical Application Circuit

The circuit of Figure 9 takes an input voltage between 3 V and 40 V and regulates it down while delivering up to 8 A of load current.

SETTING THE OUTPUT VOLTAGE

Based on the circuit of Figure 9, the output voltage depends on the feedback voltage V_{FB} and the resistor divider network consisting of R3 and R4, as expressed with the following equation:

$$V_{OUT} = V_{FB} \cdot \frac{R_3 + R_4}{R_4}$$

The R4 resistor value may be as high as 100 kΩ, however 10 kΩ resistor value is typically recommended. Given this and the typical V_{FB} of 0.8 V, the R3 resistor may easily be calculated for a desired output voltage. Table 1 exemplifies several standard resistor values needed to achieve desired output voltage. If standard resistor values are not available a parallel combination of two standard resistors may also be used.

V_{OUT} [V]	R3 [kΩ]	R4 [kΩ]
1.0	2.5	10
1.2	5.0	10
1.8	12.5	10
2.5	21.25	10
3.3	31.25	10
5	52.5	10

Table 1. Examples of R3/R4 for Typical Output Voltages

SETTING THE SWITCHING FREQUENCY AND THE CURRENT LIMIT

The switching frequency is set by the resistor R1 and the cycle-by-cycle peak current limit by the resistor R2. The needed resistor values are expressed with the following equations:

$$R_1 = \frac{10\ \text{MHz}}{f_s}\ \text{k}\Omega \qquad f_s = \frac{10\ \text{k}\Omega}{R_1}\ \text{MHz}$$

$$R_2 = \frac{200\ \text{A}}{I_{lim}}\ \text{k}\Omega \qquad I_{lim} = \frac{200\ \text{k}\Omega}{R_2}\ \text{A}$$

SWITCHING FREQUENCY SYNCHRONISATION

The SPPL14080RH has a feature for synchronisation to a clock signal applied externally to the SYNC* pin. A precise frequency setting resistor R1 at ROSC pin is mandatory for this. The R1 resistor value shall be exactly calculated to match the frequency of the applied synchronisation clock signal. The synchronisation will work, when the frequency of the applied synchronisation clock is within ±10% of the nominal value used for the calculation. The SPPL14080RH synchronises to the falling edge of the applied synchronisation clock signal, which starts $t_{off,min}$.

COMPONENT SELECTION

Inductor: The operation frequency of the SPPL14080RH allows the use of small surface mount inductors. The minimum inductance value is inversely proportional to the operating frequency and is bounded by the following limits:

$$L = \frac{V_{OUT} \cdot (V_{VIN} - V_{OUT})}{f_S \cdot \Delta I_{L(MAX)} \cdot V_{VIN}} [H]$$

where

- f_S = Operating frequency [Hz]
- $\Delta I_{L(MAX)}$ = Allowable max inductor current ripple [A]
- V_{VIN} = Input voltage [V]
- V_{OUT} = Output voltage [V]

The inductor current ripple is typically set to 10% to 40% of the maximum load current. Given this, the operating frequency and the input and output voltages for the SPPL14080RH regulator circuit, it is easy to calculate the optimal inductor value. Note that a larger value inductor will result in less ripple current and ultimately in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current is given in the following equation:

$$I_{L(peak)} = I_{LOAD} + \frac{V_{OUT} \cdot (V_{VIN} - V_{OUT})}{2 \cdot f_S \cdot L_1 \cdot V_{VIN}} [A]$$

For high efficiency, it is recommended to select an inductor with a high frequency core material (e.g. ferrite) to minimize core losses. Low ESR (equivalent series resistance) is another preferred inductor characteristic when designing for low losses. The inductor must handle the peak inductor current at full load without saturating. Note that the peak inductor current must be below the maximum switch current limit. Chip inductors typically do not have enough core to support the peak inductor currents above 1 A and are not suitable for the SPPL14080RH applications.
Lastly, select a toroid, pot core or shielded bobbin inductor for low radiated noise.

Input Capacitor: The input current to the buck regulator is discontinuous, therefore, a capacitor is required to supply AC current to the regulator while maintaining the DC input voltage.
The input capacitor of Figure 9 (C1) absorbs the input switching current, therefore, it requires adequate ripple current rating. The RMS current in the input capacitor can be estimated using the following equation:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{VIN}} \cdot \left(1 - \frac{V_{OUT}}{V_{VIN}}\right)}$$

The worst case condition occurs when V_{VIN} is twice the value of V_{OUT}. In this case, the I_{C1} is equal to the half of the load current. As a rule of thumb, select the input capacitor with the RMS current rating greater than the half of the maximum load current.
The input capacitor reduces peak currents drawn from the input source and reduces input switching noise. The input voltage ripple caused by the input capacitor can be estimated using the following equation:

$$dV_{VIN} = \frac{I_{LOAD}}{C_1 \cdot f_S} \cdot \frac{V_{OUT}}{V_{VIN}} \cdot (1 - \frac{V_{OUT}}{V_{VIN}})$$

The input capacitor values in the range between 10 µF and 100 µF are sufficient in most cases. Low ESR capacitors are recommended for a low loss operation. Ceramic capacitors with X5R or X7R dielectrics are preferred, however, tantalum and electrolytic capacitors are acceptable as well. When using electrolytic or tantalum capacitors, a small (e.g. 0.1 µF) ceramic capacitor should also be used and placed as close to the VIN pin as possible.
Additional attention should be paid to the stability margin. Especially if a LC filter is used at the input, this filter should be sufficiently damped.

Output Capacitor: The value of the output capacitor of Figure 9 (C8) has an effect on the output voltage ripple as expressed in the following equation:

$$dV_{OUT} = \frac{V_{OUT}}{f_S \cdot L_1} \cdot (1 - \frac{V_{OUT}}{V_{VIN}}) \cdot (ESR_{C8} + \frac{1}{8 \cdot f_S \cdot C_8})$$

where

- f_S = Operating frequency [Hz]
- ESR_{C8} = Equivalent series resistance of C8
- V_{VIN} = Input voltage [V]
- V_{OUT} = Output voltage [V]

The output capacitor C8 can be ceramic, tantalum or electrolytic type. When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, therefore, the above equation may be simplified as the following:

$$dV_{OUT} = (1 - \frac{V_{OUT}}{V_{VIN}}) \cdot \frac{V_{OUT}}{8 \cdot f_S^2 \cdot C_8 \cdot L_1}$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency, therefore, the original output voltage ripple equation can be re-written as the following expression:

$$dV_{OUT} = \frac{V_{OUT}}{f_S \cdot L_1} \cdot \left(1 - \frac{V_{OUT}}{V_{VIN}}\right) \cdot ESR_{C8}$$

To provide low output voltage ripple a minimum output capacitor value of 40 μF is recommended.

Compensation Components: The SPPL14080RH employs current mode control for easy compensation and fast transient response. System stability and transient response are controlled via COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series RC network (C4 and R5 of Figure 9) sets a pole-zero combination and controls the characteristics of the control system. The DC gain of the voltage feedback loop is given by the following equation:

$$A_{VDC} = R_{LOAD} \cdot G_{CS} \cdot A_{EA} \cdot \frac{V_{FB}}{V_{OUT}}$$

where

- G_{CS} = Current sense transconductance [A/V]
- A_{EA} = Error amplifier voltage gain [V/V]

The system has two poles of importance. One is due to the compensation capacitor (C4 of Figure 9) and the output resistance of the error amplifier. The other one is due to output capacitor (C8 of Figure 9) and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \cdot C_4 \cdot A_{EA}}$$

$$f_{P2} = \frac{1}{2\pi \cdot C_8 \cdot R_{LOAD}}$$

where

- G_{EA} = Error amplifier transconductance [A/V]

The system has one zero of importance, due to the compensation capacitor (C4) and the compensation resistor (R5). The zero is located at:

$$f_{Z1} = \frac{1}{2\pi \cdot C_4 \cdot R_5}$$

The system may also have another zero of importance due to high output capacitance and ESR of C8 (output capacitor of Figure 9). The zero is located at:

$$f_{Z2} = \frac{1}{2\pi \cdot C_8 \cdot ESR_{C8}}$$

The C6 may be added to compensate for the ESR of C8. The C6 together with R5 creates another pole which is located at:

$$f_{P3} = \frac{1}{2\pi \cdot C_6 \cdot R_5}$$

The aim of the compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system to be unstable. As a rule of thumb, the crossover frequency (f_C) below one tenth of the switching frequency is recommended. This is expressed by the following inequality:

$$f_c < \frac{f_s}{10}$$

The following steps may be used for optimizing the compensation components:

1. Select the compensation resistor, R5 to set the desired crossover frequency. The R5 resistor value can be determined using the following equation:

$$R_5 = \frac{2\pi \cdot C_8 \cdot f_c}{G_{EA} \cdot G_{CS}} \cdot \frac{V_{OUT}}{V_{FB}}$$

2. Select the compensation capacitor C4 to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, below one quarter of the crossover frequency provides sufficient phase margin. The C4 capacitor value can be determined using the following inequality:

$$C_4 > \frac{4}{2\pi \cdot R_5 \cdot f_c}$$

3. Determine if the second compensation capacitor, C6, is needed. It is needed if the ESR zero (f_{Z2}) of the output capacitor (C8) is located at less than half of the switching frequency as expressed in the following inequality:

$$\frac{f_s}{2} > \frac{1}{2\pi \cdot C_8 \cdot ESR_{C8}}$$

If the above inequality is valid, add the second compensation capacitor, C6, to set the third pole, f_{P3}, at the location of the ESR zero, f_{Z2}. The C6 capacitor value can be determined using the following equation:

$$C_6 = \frac{C_8 \cdot ESR_{C8}}{R_5}$$

Slope Compensation: To prevent subharmonic oscillations at duty cycles D > 50% a slope compensation ramp must be set by the capacitor C5. In buck application the duty cycle is usually determined as

$$D = \frac{V_{OUT}}{V_{VIN}}$$

but some margin for regulation should be included.

To guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of current waveform. This is the case, if

$$D < 1 - \frac{1}{2} \cdot \frac{\Delta I_L}{\Delta V_S \cdot G_{CS}}, \quad \Delta V_S = \frac{I_{SLOPE}}{f_s \cdot C5}$$

where

- ΔI_L = Inductor current ripple [A]
- ΔV_S = Voltage swing of the slope compensation ramp over one switching period duration [V]
- I_{SLOPE} = Slope current [A]

Accordingly the selected C5 value must satisfy:

$$C_5 < \frac{2 \cdot (1 - D) \cdot G_{CS} \cdot I_{SLOPE}}{f_s \cdot \Delta I_L}$$

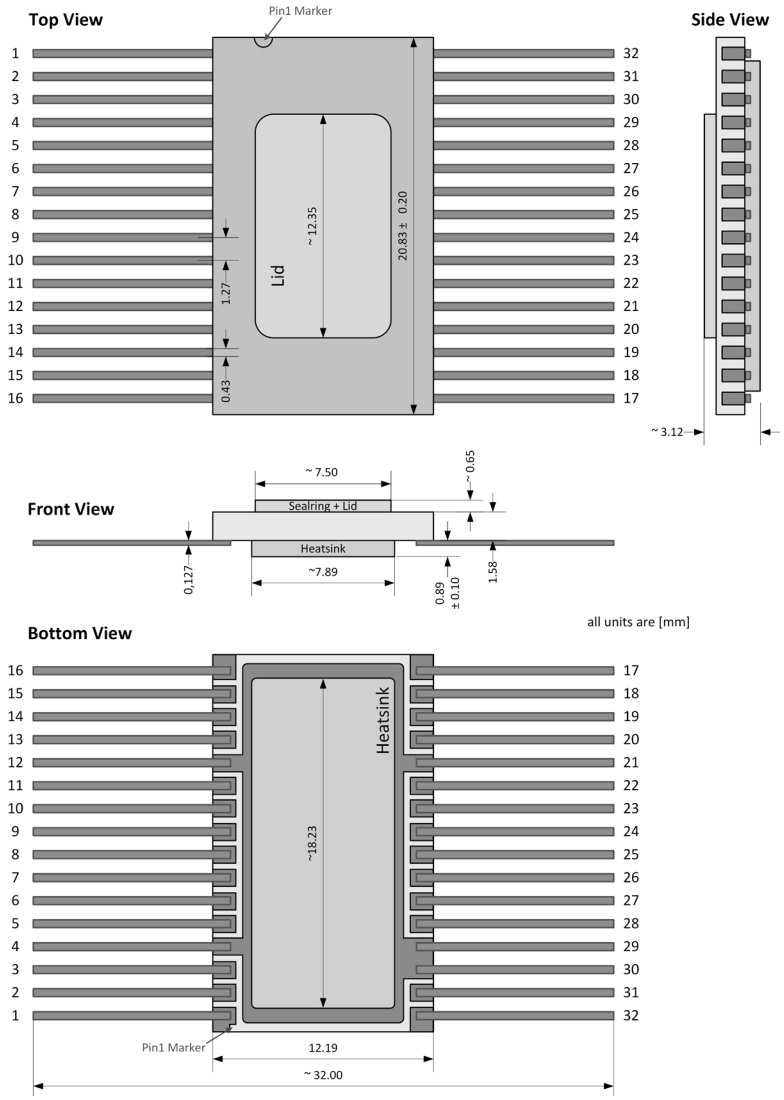
The slope capacitor C5 should be selected in the range from 10pF to 1nF. At duty cycles D ≤ 50% the slope compensation ramp can be set to 0 by shorting the pins COMP and SLOPE. Nevertheless, for better regulation behaviour (i.e. stability margin) the use of a slope compensation ramp with $\Delta V_S \geq 100mV$ is strongly recommended. The maximum ΔV_S is generally limited to 2V.

Nominal Operating Range: The need for slope compensation limits the maximum duty cycle of the application. Besides this, the duty cycle is also limited by timing parameters expressed as minimum on time $t_{ON,min}$ and minimum off time $t_{OFF,min}$:

$$f_s \cdot t_{ON,min} < D < \left(1 - f_s \cdot t_{OFF,min}\right)$$

Some margin for regulation should always be included. Consequently, this duty cycle limitation also limits the minimum and maximum conversion rate depending on the frequency. The smallest range of the duty cycle (respectively conversion rate) corresponds to the highest operating frequency, the widest range to the lowest operating frequency. This means, that not all combinations of V_{VIN}, V_{OUT} and operating frequency f_s can be realised in application. In addition, the applications with small duty cycle have the disadvantage to be more sensitive against phase jitter.

PACKAGE DIMENSION (32-LEAD FLATPACK)



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